

DOCUMENT-IDENTIFIER: US 5761517 A

TITLE: System and method for reducing power consumption in high frequency clocked circuits

DEPR:

Further, if the power.sub.-- high signal remains active through another predetermined sampling period, the control state machine sends appropriate select signals to the pattern generator and a 0001 bit pattern is output such that 0100 is loaded into the shift register, thereby reducing the system clock frequency to 25% of the oscillator clock frequency, since the inverting registers cause a 0001 to be ANDed with the oscillator clock signal. If necessary, a level 0 state could be reached which would completely turn off the system clock. That is, a 0000 bit pattern would be output and a 0101 presented to the shift register by the pattern generator wherein a 0000 will be ANDed with the oscillator clock. Various state levels 0 through 4 present the opportunity by the present invention to generate a control signal to a power supply which in response may lower the power supply voltage.

CCOR:

713/322

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Pending Active

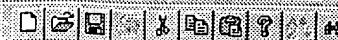
- L1: (1743) ("713/300-340").CCLS.
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- L3: (1341) (("327/113") or ("327/544")).CCLS.
- L4: (3807) 1 or 2 or 3
- L5: (1194951) frequency
- L6: (1399297) voltage
- L7: (242078) 5 same 6
- L8: (16016) state adj machine
- L9: (143) 8 same 7
- L10: (2) 9 and 4
- L11: (4146) application adj (load or demand)
- L12: (0) 11 same 9
- L14: (0) 13 and 4
- L13: (70) 11 same 7
- L15: (49824) (adjust\$ or select\$) adj2 5
- L16: (46835) (adjust\$ or select\$) adj2 6
- L17: (830) 15 same 16
- L18: (10) 17 and 4

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U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
1	<input checked="" type="checkbox"/>	US 6141762 A	20001031	9	Power reduction in a multiprocessor digital	713/300	709/100 ; 713/320
2	<input checked="" type="checkbox"/>	US 6114888 A	20000905		Digital phase lock loop divider cycling method,	327/157	327/147 ; 327/148
3	<input checked="" type="checkbox"/>	US 5974556 A	19991026		Circuit and method for controlling power and	713/322	327/509 ; 327/512
4	<input checked="" type="checkbox"/>	US 5938769 A	19990817		CPU escalating adapter with multivoltage and multiple	713/300	
5	<input checked="" type="checkbox"/>	US 5812860 A	19980922		Method and apparatus providing multiple voltages	713/322	327/113 ; 331/143

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- L14: (0) 13 and 4
- L13: (70) 11 same 7

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1	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6188585 B1	20010213	13	DC power supply apparatus	363/17	363/41 ; 363/98
2	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6152699 A	20001128		Cooling apparatus for electrical equipment	417/12	417/326 ; 417/423.1
3	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6133701 A	20001017		Driving circuit for oscillatory actuator	318/114	318/129 ; 318/130
4	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 6091049 A	20000718		Power supply apparatus for use with arc utilizing	219/130.21	219/130.32
5	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5982812 A	19991109		Method and apparatus for monitoring frequency	375/215	331/1R ; 455/192.1
6	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5959853 A	19990928		Closed-loop switched capacitor network power	363/59	
7	<input checked="" type="checkbox"/>	<input type="checkbox"/>	US 5929610 A	19990727		Method and apparatus for	322/37	318/153

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9 and 4

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1	<input type="checkbox"/>	<input type="checkbox"/>	US 5812860 A	19980922	8	Method and apparatus providing multiple voltages	713/322	327/113 ; 331/143
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5761517 A	19980602	12	System and method for reducing power consumption	713/322	713/501

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